SIES Graduate School of Technology
Nerul, Navi Mumbai

Institution's Innovation Council (IIC) of SIES GST

Event Report

Design and realization of Digital system on FPGA platform using Verilog

Event Information
Event Type: Value added Course with Internship
Event title: **Design and realization of Digital system on FPGA platform using Verilog**
Resource Person: Dr.Preeti Hemnani , Prof. Pranavi Nikam
Event date: from:8/12/2025 to 30/12/2025
Organized for:Students of SIES Graduate school of Technology , Navi Mumbai
Organized by:Department of Electronics and Telecommunication
Target audience (branch & nos.): SE/ TE/ BE students
Attachments: **List of students with internship Projects completed by the students** **2. Attendance report** **3. Feedback** **4. Certificate, Photographs (in JPEG/PNG)**

Event Description

EXTC department faculties have conducted 21 days student development program on "**Design and realization of Digital system on FPGA platform using Verilog**" followed by internship and projects. Program was conducted by Prof. Pranavi Nikam and Prof. Dr. Preeti Hemnani.

Objective of the workshop was to bridge the gap between industry requirements and academic.

23 students attended the course and successfully developed and submitted project .

Students completed their projects during online internship by SIESGST.

Certificates were given to students on successful completion and presentation of developed applications. Feedback was collected and overall feedback shows students were satisfied with content.

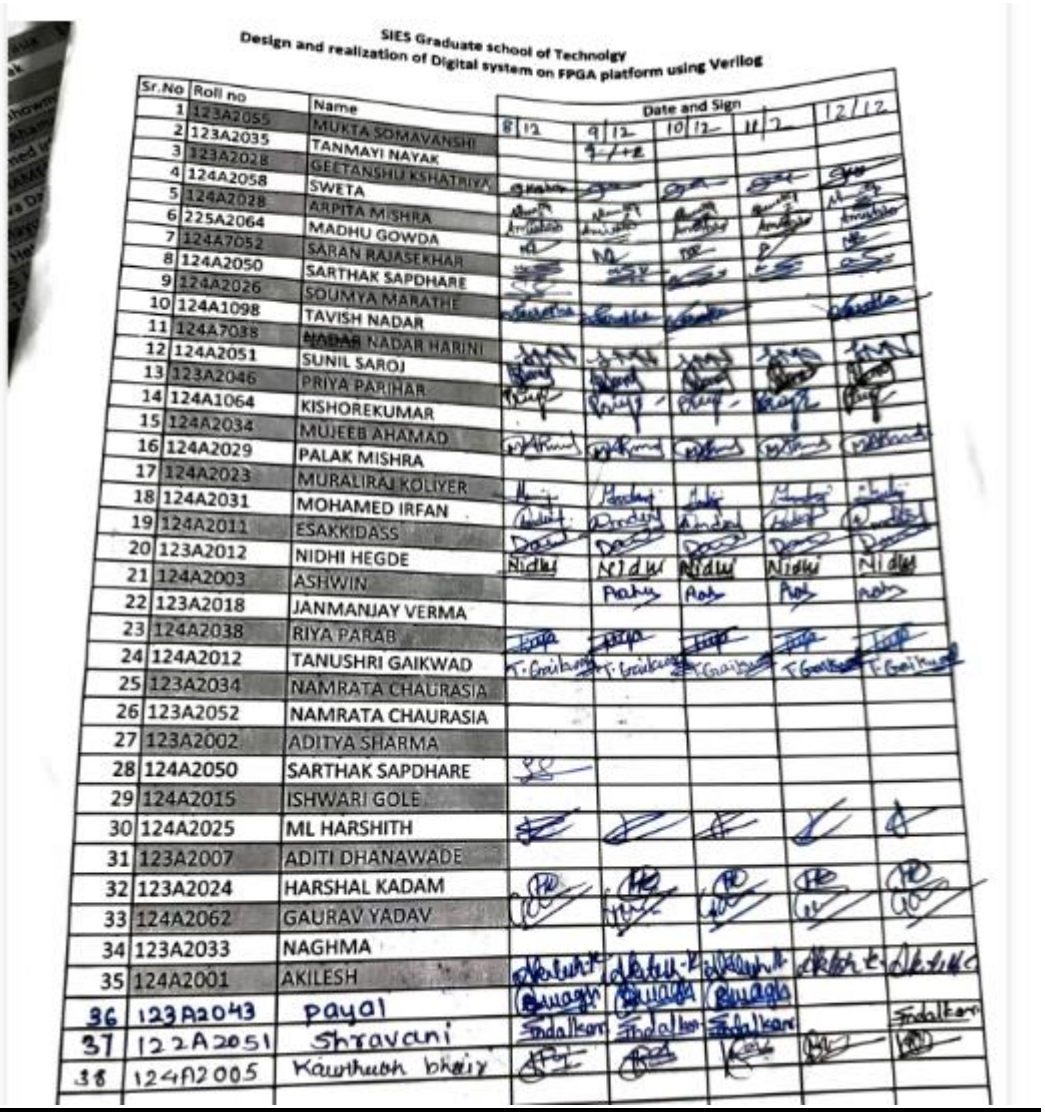
- **List of students with internship Projects completed by the students**

Sr. No	Students name	Class	Project Title
1	GEETANSHU KSHATRIYA	TE	FPGA Implementation of a Carry-Skip Adder Using Verilog HDL
2	SWETA	SE	FPGA-Based Verilog Design of an Elevator Control System with State-Machine Architecture
3	ARPITA MISHRA	SE	FPGA-Based Verilog Design of an Elevator Control System with State-Machine Architecture
4	MADHU GOWDA	SE	FPGA-Based Verilog Design of an Elevator Control System with State-Machine Architecture
5	SARAN RAJASEKHAR	SE	FPGA-Based Digital Lock System Design Using Verilog HDL

6	SARTHAK SAPDHARE	SE	Not completed
7	SOUMYA MARATHE	SE	Secure FPGA-Based Electronic Voting Machine Design Using Verilog HDL
8	NADAR HARINI MADHAVAN	SE	FPGA-Based Digital Lock System Design Using Verilog HDL
9	SUNIL SAROJ	SE	Design and FPGA Implementation of Traffic Light Controller Using Verilog HDL
10	PRIYA PARIHAR	TE	FPGA-Based Verilog Implementation of an Automated Soda Dispenser Control System
11	MUJEEB AHAMAD	SE	Design and FPGA Implementation of a Smart Car Parking Slot Management System Using Verilog
12	MURALIRAJ KOLIYER	SE	Design and FPGA Implementation of a Smart Car Parking Slot Management System Using Verilog
13	MOHAMED IRFAN	SE	Design and FPGA Implementation of a Smart Car Parking Slot Management System Using Verilog
14	ESAKKIDASS	SE	Design and FPGA Implementation of a Smart Car Parking Slot Management System Using Verilog
15	NIDHI HEGDE	TE	FPGA-Based Verilog Implementation of an Automated Soda Dispenser Control System
16	ASHWIN	SE	FPGA-Based Verilog Design of an Elevator Control System with State-Machine Architecture
17	RIYA PARAB	SE	Secure FPGA-Based Electronic Voting Machine Design Using Verilog HDL
18	TANUSHRI GAIKWAD	SE	Not Completed

19	ML HARSHITH	SE	Secure FPGA-Based Electronic Voting Machine Design Using Verilog HDL
20	HARSHAL KADAM	TE	FPGA Implementation of a Carry-Skip Adder Using Verilog HDL
21	GAURAV YADAV	SE	Secure FPGA-Based Electronic Voting Machine Design Using Verilog HDL
22	AKILESH	SE	FPGA-Based Digital Lock System Design Using Verilog HDL
23	Payal Wagh	TE	FPGA-Based Verilog Implementation of an Automated Soda Dispenser Control System
24	Shravani Indulkar	TE	FPGA-Based Verilog Implementation of an Automated Soda Dispenser Control System
25	Kaushtubh Bhoir	SE	Design and FPGA Implementation of Traffic Light Controller Using Verilog HDL

Attendance :



SIES Graduate school of Technolgy

Design and realization of Digital system on FPGA platform using Verilog

Sr.No	Roll no	Name	Date and Sign				
			8/12	9/12	10/12	11/12	12/12
1	123A2055	MUKTA SOMAVANSHI					
2	123A2035	TANMAYI NAYAK					
3	123A2028	GEETANSHU KSHATRIYA					
4	124A2058	SWETA					
5	124A2028	ARPITA MISHRA					
6	225A2064	MADHU GOWDA					
7	124A7052	SARAN RAJASEKHAR					
8	124A2050	SARTHAK SAPDHARE					
9	124A2026	SOUMYA MARATHE					
10	124A1098	TAVISH NADAR					
11	124A7038	NADAR NADAR HARINI					
12	124A2051	SUNIL SAROJ					
13	123A2046	PRIYA PARIHAR					
14	124A1064	KISHOREKUMAR					
15	124A2034	MUJEEB AHAMAD					
16	124A2029	PALAK MISHRA					
17	124A2023	MURALIRAJ KOLIYER					
18	124A2031	MOHAMED IRFAN					
19	124A2011	ESAKKIDASS					
20	123A2012	NIDHI HEGDE	Nidhi	Nidhi	Nidhi	Nidhi	Nidhi
21	124A2003	ASHWIN		Ashy	Ash	Ash	Ashy
22	123A2018	JANMANJAY VERMA					
23	124A2038	RIYA PARAB					
24	124A2012	TANUSHRI GAIKWAD	T. Gaikwad	T. Gaikwad	T. Gaikwad	T. Gaikwad	T. Gaikwad
25	123A2034	NAMRATA CHAURASIA					
26	123A2052	NAMRATA CHAURASIA					
27	123A2002	ADITYA SHARMA					
28	124A2050	SARTHAK SAPDHARE					
29	124A2015	ISHWARI GOLE					
30	124A2025	ML HARSHITH					
31	123A2007	ADITI DHANAWADE					
32	123A2024	HARSHAL KADAM					
33	124A2062	GAURAV YADAV					
34	123A2033	NAGHMA					
35	124A2001	AKILESH					
36	123A2043	payal	Bhagat	Bhagat	Bhagat		
37	122A2051	Shravani	Indalkar	Indalkar	Indalkar		Indalkar
38	124A2005	Kawthuoh bhoiy					

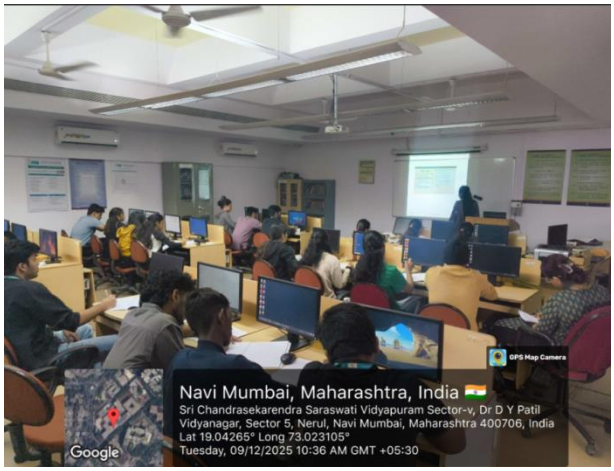
SIES Graduate school of Technology

Design and realization of Digital system on FPGA platform using Verilog

Project internship

Sr.No	Roll no	Name	Date and Sign				
1	123A2055	MUKTA SOMAVANSHI					
2	123A2035	TANMAYI NAYAK					
3	123A2028	GEETANSHU KSHATRIYA					
4	124A2058	SWETA					
5	124A2028	ARPITA MISHRA					
6	225A2064	MADHU GOWDA					
7	124A7052	SARAN RAJASEKHAR					
8	124A2050	SARTHAK SAPDHARE					
9	124A2026	SOUMYA MARATHE					
10	124A1098	TAVISH NADAR					
11	124A7038	NADAR NADAR HARINI					
12	124A2051	SUNIL SAROJ					
13	123A2046	PRIYA PARIHAR					
14	124A1064	KISHOREKUMAR					
15	124A2034	MUJEEB AHAMAD					
16	124A2029	PALAK MISHRA					
17	124A2023	MURALIRAJ KOLIYER					
18	124A2031	MOHAMED IRFAN					
19	124A2011	ESAKKIDASS					
20	123A2012	NIDHI HEGDE					
21	124A2003	ASHWIN					
22	123A2018	JANMANJAY VERMA					
23	124A2038	RIYA PARAB					
24	124A2012	TANUSHRI GAIKWAD					
25	123A2034	NAMRATA CHAURASIA					
26	123A2052	NAMRATA CHAURASIA					
27	123A2002	ADITYA SHARMA					
28	124A2050	SARTHAK SAPDHARE					
29	124A2015	ISHWARI GOLE					
30	124A2025	ML HARSHITH					
31	123A2007	ADITI DHANAWADE					
32	123A2024	HARSHAL KADAM					
33	124A2062	GAURAV YADAV					
34	123A2033	NAGHMA					
35	124A2001	AKILESH					
36	123A2043	Payal					
37	122A2051	Shravani					
38	12A2005	Kaushtubh					

- **Photographs (in JPEG/PNG)**



Feed back :

A	B	C	D	E	F	G	H	I	J	K
ID	Name	Branch	Are you able to understand basic of FPGA and Verilog Coding ?	Are you able to understand combinational circuit execution	Are you able to understand Sequential circuit execution?	Are you able to understand FSM execution ?	Content Delivery by Speakers	How relevant you think it was for your future	Effectiveness of SDP	Any other suggestion or Your views about Value added course
1	MUJEEB AHAMAD	EXTC	5	4	5	4	4	5	5	Nothing
2	PAYAL WAGH	EXTC	5	5	5	5	5	5	5	no
3	NADAR NADAR HARINI MADHAVAN	ECS	5	5	5	5	5	5	5	None
4	AKILESH	EXTC	5	5	5	5	5	5	5	Nil
5	PRIYA PARIHAR	EXTC	4	4	4	5	5	4	5	nil
6	ESAKKIDASS	EXTC	4	4	4	4	5	4	3	I learned about how to use FPGA board using verilog.
7	Kausthubh Bhoir	EXTC	5	5	5	5	5	5	5	No
8	HARSHAL KADAM	EXTC	5	4	5	4	5	5	5	NULL
9	SHRAVANI INDALKAR	EXTC	5	5	4	5	5	5	5	NA

➢ Impact Analysis-

The session inspired curiosity and creativity among students, improved their confidence, and motivated them to work on FPGA and participate in Technical Competition.

➢ Certificate :

SIES Graduate School of Technology (Autonomous)
RISE WITH EDUCATION
NAAC A+

EXTC/FPGA/DEC25/03

CERTIFICATE

OF COMPLETION

THIS IS TO CERTIFY THAT

ARPITA MISHRA

has successfully completed the Value Added Course on "**Design and Realization of Digital Systems on FPGA Platform Using Verilog**".
and followed an in-house internship from 8/12/2025 to 30/12/2025, Organized by Electronic and Telecommunication Department SIES GST, During the internship, he/she completed the project titled "**FPGA-Based Verilog Design of an Elevator Control System with State-Machine Architecture**"

Head of the D al

6 / 25